IN THE CLAIMS:

Please amend claims 9, 14, 20, 21 and 29, add claims 30-33 and cancel claim 28 as follows.

Claims 1-8. (Cancelled)

9. (Currently Amended) A method for improving the reliability of a computer system including a bus, at least one ~~and~~ plug-in unit and at least one separate interface circuit corresponding to each of the at least one plug-in unit ~~units coupled thereto~~, comprising:

connecting at least one plug-in unit to ~~a~~ the bus via ~~a~~ the separate interface circuit ~~corresponding thereto~~;

addressing a respective plug-in unit, via the bus, by addressing operations directed at said respective plug-in unit and which are monitored locally by ~~said~~ the corresponding interface circuit of the respective plug-in unit ~~corresponding thereto~~;

performing a time duration operation of addressing of said plug-in unit; and

checking the state of addressing of the addressed plug-in unit such that (i) when the addressing is ended before expiration of a predetermined period of time, the time duration operation of addressing is terminated and a new time duration operation of addressing is set to commence at time of next occurrence of addressing, and (ii) when the duration operation of addressing exceeds the predetermined time period, the addressing to

that plug-in unit is terminated by ~~said~~ the corresponding interface circuit ~~corresponding thereto~~ by sending into the bus a signal indicating termination of addressing.

10. (Previously Presented) A method as defined in claim 9, wherein:

the time duration of addressing is monitored using a watchdog timer with a predetermined timing set therein.

11. (Previously Presented) A method as defined in claim 9, wherein:

when addressing is terminated an error signal is set by the interface circuit into an active state in the bus.

12. (Previously Presented) A method as defined in claim 9, wherein:

when addressing is terminated an error signal indicating an error condition in the plug-in unit is set by the interface circuit into an active state in the status register of the plug-in unit.

13. (Previously Presented) An interface circuit for providing local monitoring capability to a plug-in unit of a computer system, comprising:

a watchdog timer;

first means for activating the watchdog timer upon start of an addressing operation directed to the plug-in unit corresponding thereto; and

second means for sending into a bus a signal indicating termination of addressing, the termination of addressing being effected when the duration of said addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer.

14. (Currently Amended) An interface circuit as defined in claim 13, further comprising:

means for setting an error signal into an active state in ~~a~~ the bus.

15. (Previously Presented) An interface circuit as defined in claim 13, further comprising:

means for setting a signal indicating an error condition in a plug-in unit into an active state in a status register of the plug-in unit.

16. (Previously Presented) An interface circuit as defined in claim 14, further comprising:

means for setting a signal indicating an error condition in a plug-in unit into an active state in a status register of the plug-in unit.

17. (Previously Presented) An interface circuit as defined in claim 13, wherein:

the bus is a Compact PCI bus.

18. (Previously Presented) An interface circuit as defined in claim 16, wherein: the bus is a Compact PCI bus.

19. (Cancelled)

20. (Currently Amended) A method according to claim 10, wherein:

said watchdog timer is provided at each ~~said~~ interface circuit ~~or at each of at least one plug-in unit~~.

21. (Currently Amended) A computer system including a bus, ~~and~~ at least one plug-in unit and at least one separate interface circuit corresponding to each of the at least one plug-in unit ~~units coupled thereto~~, wherein the computer system comprises:

at least one separate interface circuit correspond to each of the at least one plug-in unit where each plug-in unit ~~a plurality of interface circuits and a plurality of plug-in units each of which~~ is connected to said bus via ~~a~~ the separate one of said interface circuits ~~further corresponding thereto~~, wherein each of said interface circuits comprises:

a watchdog timer;

first means for activating the watchdog timer upon start of an addressing operation directed to the corresponding plug-in unit ~~corresponding thereto~~; and

second means for sending into the bus a signal indicating termination of addressing, the termination of addressing being effected when the duration of said

addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer.

22. (Previously Presented) A computer system according to claim 21, wherein each said interface further comprises:

means for setting an error signal into an active state in the bus.

23. (Previously Presented) A computer system according to claim 22, wherein each said interface circuit comprises:

means for setting a signal indicating an error condition in the corresponding plug-in unit into an active state in a status register of the plug-in unit.

24. (Previously Presented) A computer system according to claim 23, wherein:

the bus is a Compact PCI bus.

25. (Previously Presented) A computer system according to claim 21, wherein each said interface circuit comprises:

means for setting a signal indicating an error condition in the corresponding plug-in unit into an active state in a status register of the plug-in unit.

26. (Previously Presented) A computer system according to claim 21, wherein:

the bus is a Compact PCI bus.

27. (Cancelled)

28. (Cancelled)

29. (Currently Amended) An interface circuit for providing local monitoring capability to a plug-in unit of a computer system, comprising

a bus and plug-in units ~~coupled~~ connected to the bus via ~~; a~~ separate interface circuits, thereby ~~circuit~~ connecting each ~~of the~~ plug-in unit ~~units~~ to the bus;

a watchdog timer;

an activating device configured to activate the watchdog timer upon start of an addressing operation directed to the corresponding plug-in unit ~~corresponding thereto~~; and

a sending device configured to send a signal into the bus indicating termination of addressing, the termination of addressing being effected when the duration of said addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer.

30. (New) An interface circuit as defined in claim 29, further comprising a device configured to set a signal indicating an error condition in a plug-in unit into an active state in a status register of the plug-in unit.

31. (New) An interface circuit as defined in claim 29, wherein:

the bus is a Compact PCI bus.

32. (New) An interface circuit as defined in claim 30, wherein:

the bus is a Compact PCI bus.

33. (New) An interface circuit as defined in claim 29, further comprising a device for setting an error signal into an active state in a bus.